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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/353,120	07/14/1999	LOUIS F. VILLAROSA JR.	061607-1100	3012

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EXAMINER
KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/353,120	VILLAROSA ET AL.	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 10-13* is/are rejected.

7)☒ Claim(s) *5 and 14-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 1-7 and 10-26 have been considered but are moot in view of the new ground(s) of rejection. Claims 8 and 9 have been cancelled.

Response to Amendment

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2, 3, 4, 11, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamane et al. USPN 4965797.

1. Regarding claim 1, Yamane shows in figure 4, a circuit for detecting errors in the synchronization of a DTE data signal (Yamane fig. 10: output of 49) with a DCE clocking signal

(Yamane fig. 4: input clock) in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

a. a master clock producing a master clock signal (Yamane fig. 4: multiple clock; fig. 10: phi3) having a frequency that is an integer multiple of the frequency of the DCE clocking signal (Yamane fig. 4: input clock; fig. 9 shows multiple clock phi3 is at twice the frequency of the input clock; fig. 10 shows input clock phi0 is at fo while phi3 is at 2fo).

b. a clock generator deriving (Yamane fig. 4: Divider 34) a circuit clocking signal (Yamane fig. 4: bottom output of divider 34; fig. 10: phi1) from said master clock signal (Yamane fig. 4: multiple clock), said circuit clocking signal (Yamane fig. 11: f divided clock) having the same frequency as the DCE clocking signal (Yamane fig. 11: a input clock; in fig. 11, a and f are at the same frequency).

c. a sample enable generator (Yamane fig. 10: 28) for generating a first sample enable signal (Yamane fig. 10: sel1) at a first time related to said circuit clocking signal and a second sample enable signal (Yamane fig. 10: sel2) at a second time related to said master clock signal (master clock, which is the output of 33, is related to the circuit clock, which is the output of 34, and both are used to obtain the sample enable signals); and

d. a sample comparator for using said first sample enable signal, said second enable signal and said DTE data signal to determine whether the DTE data signal has undergone a transition during the time interval between said first time and said second time (Yamane fig. 10: comparison of samples is occurring in 49 with the NAND gates).

2. Regarding claim 2, Yamane shows the circuit of claim 1 wherein the frequency of said master clock signal (Yamane fig. 4: multiple clock) is approximately 8 times the frequency of said DCE clocking signal (Yamane fig. 4: input clock). Yamane shows in fig. 9 that multiple clock phi3 is twice (which is approximately 8 times) the frequency of the input clock phi0.

3. Regarding claim 3, Yamane shows the circuit of claim 1 wherein the time interval between said first time and said second time (Yamane shows this in fig. 11 b and c with D1 and d1 since they are output based on sel1 and sel2, respectively) is approximately 1/8 of the period of said DCE clocking signal (Yamane fig. 11: DCE clocking signal is in 11a with input clock phi0. The period between D1 and d1 in 11b and 11c, as can be seen with the start of D(0) is ¼ of the period of phi0 and ¼ is approximately 1/8.)

4. Regarding claim 4, Yamane shows the circuit of claim 1 wherein said sample comparator (Yamane fig. 10: 49) generates a selector control signal (Yamane fig. 1: outputs of 49) if said first sample (Yamane fig. 10: 49: output of the NAND gate through with D1 is input) is different from said second sample (Yamane fig. 10: 49: output of the NAND gate through with D2 is input).

5. Regarding claim 11, Yamane shows a method for detecting errors in the synchronization of a DTE data signal (Yamane fig. 4: output of 31: MD1) with a DCE clocking signal (Yamane

fig. 4: input clock) in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

e. providing a master clock signal (Yamane fig. 4: multiple clock) having a frequency that is an integer multiple of the frequency of the DCE clocking signal (Yamane fig. 4: input clock; fig. 9 shows multiple clock phi3 is at twice the frequency of the input clock)

f. deriving (Yamane fig. 4: Divider 34) a circuit clocking signal (Yamane fig. 4: bottom output of divider 34) from said master clocking signal (Yamane fig. 4: multiple clock), said circuit clocking signal (Yamane fig. 11: f divided clock) having the same frequency as the DCE clocking signal (Yamane fig. 11: a input clock; in fig. 11, a and f are at the same frequency).

g. obtaining a first sample of said DTE data signal at a first time based on said circuit clocking signal (Yamane fig. 11m: D(0))

h. obtaining a second sample of said DTE data signal at a second time based on said master clocking signal (Yamane fig. 11m: D(1)), said second time being subsequent to said first time (Yamane fig. 11m: D(1) is after D(0)), the interval between said first time and said second time being less than the period of the DCE clocking signal (Yamane fig. 11 m, n, a: the clock for clocking the MD1 data in m is in n which is at twice the frequency of the input clock, a, which is the DCE clocking signal)

i. comparing said first sample to said second sample (Yamane fig. 8: comparison of samples is occurring in 31 with the NAND gates)

6. Claims 12 and 13 have been discussed above with Yamane.

7. Claims 6, 7 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by McMahan et al. 5,870,446.

8. Regarding claim 6, McMahan et al. shows in figure 1, a circuit for detecting errors in the synchronization of a DTE data signal (McMahan 11) with a DCE clocking signal (McMahan 43 and 55) in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

j. Means for producing a master clock signal (McMahan HS CLK) having a frequency greater than the frequency of the DCE clocking signal (McMahan: At the end of the first full paragraph of column 6, it is implied that the master clock signal is 16 MHz and the DCE clocking signal is 1.544 MHz;)

k. Means for deriving a circuit clocking signal from said master clocking signal, said circuit clocking signal having the same frequency as the DCE clocking signal. (a clock generator (McMahan 55) deriving a circuit clocking signal (TX CLOCK) from said master clock signal (McMahan HS CLK input to 48), said circuit clocking signal having the same frequency as the DCE clocking signal;)

l. means for obtaining a first sample of said DTE data signal at a first time (McMahan 15) and a second sample of said DTE data signal at a second time (McMahan 15), said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal. As

indicated in the first office action, the interval between the first and second time is 1/(16 MHz), which is less than 1/(1.544MHz), the period of the DCE clocking signal

m. means for comparing said first sample to said second sample (McMahan 21)

n. means for generating a selector control signal if said first sample is different from said second sample (McMahan 23)

o. means for inverting said circuit clocking signal to produce an inverted circuit clocking signal (McMahan fig. 2: 203 and 205; col. 5 lines 55 to 60); and

p. means for selecting an output signal from the group consisting of said circuit clocking signal and said inverted circuit clocking signal (McMahan fig. 2: selects between 203 and 205) in response to said selector control signal (McMahan fig. 1: the appropriate TX CLOCK is selected in response to 23).

9. Regarding claim 7, figure 1 in McMahan et al. shows the circuit of claim 6 wherein the interval between said first time and said second time is approximately 1/8 of the period of the DCE clocking signal. The data sampling shift register (15) is sampling at 16 MHz which is approximately 1/8 of the period of the 1.544 MHz DCE clocking signal.

10. Regarding claim 10, the circuit of claim 6 further comprising means for latching said DTE data signal (inherent for data to be latched for it to be useful).

Allowable Subject Matter

11. Claims 5, 14-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. Regarding claim 5, Yamane shows the circuit of claim 4 with an inverter (Yamane fig. 10: combination of buffer 54 and delay 51 produce an inverter) producing an inverted circuit clocking signal (Yamane fig. 11d is normal phi1 and 11f is inverted phi1) from said circuit clocking signal (Yamane fig. 11d: phi1; fig. 10: phi1); and a selector (Yamane fig. 10: 31) ***producing an output signal that is selected from the group consisting of said circuit clocking signal and said inverted circuit clocking signal (not in Yamane)***, in response to said selector control signal (Yamane fig. 10: bottom input into 31)

13. As per claim 14, the method of claim 13, further comprising the steps of: inverting said circuit clocking signal to produce an inverted circuit clocking signal (discussed above); and ***producing an output signal that is selected from the group selected from said circuit clocking signal and said inverted circuit clocking signal*** (not in Yamane).

14. As per claim 23, McMahan shows the circuit of claim 10 wherein said circuit clocking signal (McMahan TX CLOCK) is used as said DCE clocking signal (McMahan TX CLOCK) and ***said obtaining means and said latching means are clocked by said output signal*** (not in McMahan).

15. As per claim 24, McMahan shows the circuit of claim 10, wherein ***said obtaining means and said latching means are clocked by said circuit clocking signal*** (not in McMahan) and said output signal is used as said DCE clocking signal (McMahan TX CLOCK).

16. Claim 15 depends on claim 14.

17. Claims 16 to 22 depend on claim 5.

18. Claims 25 and 26 depend on claim 15.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Fujii USPN 4481648

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

PK
September 12, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 9/18/02